UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,895	11/09/2001	Gurtej S. Sandhu	98-1191.01	8300

7590 12/14/2004

Charles Brantley
Micron Technology, Inc.
8000 S Federal Way
Boise, ID 83716

EXAMINER	
UMEZ ERONINI, LYNETTE T	
ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/010,895	SANDHU, GURTEJ S.	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-78* is/are pending in the application.

4a) Of the above claim(s) *17-21 and 43-58* is/are withdrawn from consideration.

5)☒ Claim(s) *59-65* is/are allowed.

6)☒ Claim(s) *22-42 and 66-78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/9/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 22-42 and 59-78 in the reply filed on 8/16/2004 is acknowledged.

Priority

2. It is suggested to update the current status of the present application.

Specification

3. The use of the trademark "Flowfill" has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 32 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 32 contains the trademark/trade name Flowfill. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe a deposition process and, accordingly, the identification/description is indefinite.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Romankiw (US 3,971,710).

As to claims 22-27, Romankiw teaches dielectric materials include glass, silicon dioxide, and conductive oxides of metals such as titanium and tantalum and may be deposit on top of a semiconductor substrate (column 3, lines 52-55 and 59-61). Romankiw also teaches a first dielectric layer **3** and a first anodized porous material-containing layer **1** (same as applicant's porous second oxide layer) on the dielectric layer (column 7, lines 18-23). The aforementioned reads on,

A method of providing oxide for an in-process semiconductor device, comprising: depositing a first oxide over said in-process semiconductor device; and depositing a porous second oxide onto said first oxide.

Romankiw differs in failing to teach non-conformally depositing a porous second oxide onto the said first oxide, **in claim 22**.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use known deposition methods of non-conformally depositing a layer on a semiconductor for the purpose of obtaining a suitable semiconductor component.

9. Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu et al. (US 5,985,770) in view of Ilg et al. (EP 875929 A2).

As to claims 28-30, Sandhu teaches a method of forming a layer comprising liquid silicon oxide precursor onto a substrate, doping the layer and transforming it into a solid doped silicon oxide containing layer on the substrate (Abstract). Sandhu further teaches doping silicon oxide with a doping gas such as PH_3, B_2H_6, F_2, NH_3, NF_3, C_2F_6, and CH_4, at temperature less than or equal to 50°C at a pressure below 100 Torr (column 2, lines 45-61 and column 3, lines 7-9); then raising the temperature of deposited liquid precursor to at least 100°C and a second temperature of at least 350°C (column 3, lines 18-27). The above reads on,

A method of providing a doped oxide, comprising: flowing an oxide precursor over a portion of a semiconductor device; forming an oxide from said precursor; and subsequently annealing said oxide.

Sandhu differs in failing to teach annealing said oxide in an atmosphere containing a dopant, **in claim 28**; and to specify the annealing temperature and time as recited in **claim 30**.

Ilg teaches a flowable oxide material **24** is ion implanted in a phosphine (PH_3) atmosphere in an oven of 400°C to 900°C for sixty minutes (column 4, lines 51-53).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Sandhu by annealing an oxide layer in an atmosphere containing a dopant as taught by Ilg for the purpose of providing gettering to remove adverse effects of alkali ion contaminant ion, which may enter the gap filling material (column 5, lines 15-23).

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 31; 34; 37-39; and 71 are rejected under 35 U.S.C. 102(b) as being anticipated by Ilg et al. (EP '929 A2).

Ilg teaches filling gaps between adjacent gate electrodes on a semiconductor structure (column 2, lines 50-52), which has a plurality of MOS transistors (column 3, lines 6-20) and which is similar to DRAM devices (column 1, lines 13-16). Ilg also teaches filling the gaps between the gate electrodes with material **24** that is a flowable oxide (column 3, lines 30-45) and ion implanting the material **24** (column 3, line 55 – column 4, line 19). The above reads on,

A method of processing a surface of an in-process memory device, comprising:

providing said surface as part of said memory device using a non-CVD process;

flowing a material onto said surface;

turning said material into a first oxide; and

doping said first oxide, **in claim 31**.

Ilg also teaches, "In one embodiment, a self-planarizing material (a flowable material, which is the same as applicants' oxide) is deposited over the structure. A first portion of such material flows between the gate electrodes to fill the gaps and a second portion of such material becomes deposited over tops of the gate electrodes and over

the gaps to form a layer with a substantially planar surface. A dopant, here phosphorous, is formed in the second portion of the self-planarizing material" (column 1, line 52 – column 2, line 1 and FIGS. 1, 2, and 3A). The aforementioned reads on,

A method of providing an etch stop for a semiconductor device, comprising:

providing at least one support surface as part of said semiconductor device, said surface having a horizontal portion and a non-horizontal portion; depositing an oxide onto said support surface, wherein said oxide has a uniform thickness on said horizontal portion and a variable thickness on said non-horizontal portion; and

doping said oxide, **in claim 34**;

introducing an impurity in said oxide, **in claim 71**;

A method of providing a CMP stop for a semiconductor device, comprising:

providing an element of said semiconductor device, said element having a top and a side;

depositing an oxide over said element, wherein said depositing leaves more of said oxide on said top than on said side; and

annealing said oxide in a doping atmosphere, **in claim 37;** and

wherein said step of depositing an oxide comprises depositing said oxide using a spin-on-glass process, **in claim 39**.

IIg further teaches the flowable oxide **24** is spun between the gaps between adjacent gate electrodes **14** and over the tops of the gate electrodes and the filled gaps (column 3, lines 38-45) and material **24** is cured at a temperature of 400 to 900 C in a nitrogen atmosphere during the ion implantation, which reads on,

wherein said step of depositing an oxide comprises: flowing a precursor to said oxide over said element; and heating said precursor, **in claim 38**.

Claim Rejections - 35 USC § 103

12. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ilg (EP '929 A2) as applied to claim 31 above.

Ilg differs in failing to teach doping a second portion of said first oxide with a second impurity.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use a conventional method of doping a layer wherein the first and second doping with a first and a second impurity, respectively for the purpose of forming source and drain of a memory device.

13. Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ilg as applied to claims 34.

Ilg differs in failing to teach,

wherein said depositing step comprises depositing said oxide by way of a CVD process, **in claim 35**;

wherein said depositing step comprises depositing said oxide by way of an HDP CVD process, **in claim 36**.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use know methods such as CVD or HDP-CVD and flowing a

precursor to said oxide in depositing an oxide layer on a semiconductor device for the purpose of obtaining a suitable semiconductor component.

14. Claims 72-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over IIg (EP '601), as applied to claim 71 above.

IIg differs in failing to teach wherein said step of providing an oxide in a non-conformal manner comprises providing an oxide having a first thickness on said higher horizontal surface, a second thickness on said lower horizontal surface, and a third thickness on said non-horizontal surface, wherein said first, second, and third thicknesses are different, in claim 72.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use conventional methods of depositing an oxide layer having a first thickness on said higher horizontal surface, a second thickness on said lower horizontal surface, and a third thickness on said non-horizontal surface, wherein said first, second, and third thicknesses are different for the purpose of obtaining a suitable semiconductor component.

Claim Rejections - 35 USC § 103

15. Claims 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder (US 5,192,706) in view of Wong et al. (US 5,946,601).

Rodder teaches a method of anisotropically depositing silicon oxide to fill trenches to produce a flat planar surface (flush with the surface of the semiconductor body) without any birds' beak (column 2, lines 45-52 and FIG. **5**).

Rodder differs in failing to teach introducing a dopant into said oxide and diffusing said dopant from said oxide into said material.

Wong teaches, "The use of low k materials have been found reduce the RC Time Constant due to a decreased capacitance. Reducing the RC Time Constant helps to increase the speed of the device. The use of low k materials have also been found to improve power dissipation and to reduce crosstalk noise between metal lines" (column 1, lines 45-51). Wong also teaches, "One way which has been found to reduce the dielectric constant of oxides, such as silicon dioxide, is to dope the oxide (column 1, lines 31-35).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Rodder by using known methods of doping an oxide as taught by Wong for the purpose of making a low dielectric material, which reduces the RC Time constant to help increase the speed of the device.

16. Claims and 66-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (US 5,897,364) in view of Kwon et al. (US 5,796,133) and Havemann (US 5,565,384).

Pan teaches depositing a BSG layer **24** over a semiconductor, which has a gate electrode **16** and dielectric side walls **22** (same as applicant's insulation layer) and

depositing a PSG layer **28** on the BSG layer **24** (column 2, lines 12-43), which reads on,

A method of depositing an interlayer dielectric, comprising:

providing a first level of a semiconductor device, said first level defining a topography and comprising insulation;

depositing BSG onto discrete portions of said topography; and

providing a second level of said semiconductor device over said BSG.

Pan differs in failing to teach said BSG having a dielectric constant of at most 3, **in claim 66**.

Kwon teaches a low dielectric material comprising BSG (column 4, lines 27-34).

Havemann teaches, ". . . Silicon dioxide has a dielectric constant of about 3.9. This constant is based on a scale where 1.0 represents the dielectric constant of a vacuum. Various materials exhibit dielectric constants from very near 1.0 to values in the hundreds. As used herein, the term low-k will refer to a material with a dielectric constant less than 3.5" (column 1, lines 56-64). Havemann also teaches low-k dielectric materials are used as a gap filler between horizontally adjacent conductors, thereby decreasing line-to-line capacitance (column 2, lines 31-36). The above reads on BSG having a dielectric constant of at most 3.

Since it is known that low k dielectric material insulate conductive material to decrease the capacitance between adjacent conductors (Havemann, column 2, lines 31-36), BSG is a low k material and low k materials have dielectric constant less than 3.5, then it would have been obvious to one having ordinary skill in the art to modify

Pan by combining the teachings of Kwon and Havemann in employing a low k material such BSG, for the purpose of decreasing the capacitance between neighboring conducting layers.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

18. Claims 42 and 77 and rejected under 35 U.S.C. 102(e) as being anticipated by Li et al. (US 6,395,647 B1).

Li teaches, ". . . liquid-containing layer **30** is formed on the substrate **10** by chemical vapor deposition through a modified form of the FLOWFILL™ process in which methyl silane (CH_3SiH_3) rather than silane is reacted with hydrogen peroxide in the chamber . . . In another embodiment, the liquid-containing layer **30** is formed by spin applying a mixture of silicon dioxide in a liquid onto the substrate **10** to form a liquid-containing layer **30** through the spin-on process. The liquid in the liquid-containing layer **30** formed by the spin-on process may be water or an organic solvent. Dopants such as arsenic, antimony, boron, phosphorus, and gallium may optionally be included in the

liquid" (column 8, lines 35-39 and 61 – column 9, line 1 and FIG. **6**). The above reads on,

A method of forming a doped oxide over a substrate, comprising:

reacting a methylsilane with hydrogen peroxide proximate said substrate; forming an oxide from a product of said methylsilane and said hydrogen peroxide; and introducing a dopant into said oxide, **in claim 77**; and

A method of filling a trench included as part of a semiconductor device, comprising:

reacting methylsilane with hydrogen peroxide in a chamber containing said semiconductor device;

allowing a product from a reaction of said methylsilane and said hydrogen peroxide to at least fill said trench;

changing said product into a silicon oxide; and

heating said silicon oxide in a boron atmosphere, **in claim 42**.

Claim Rejections - 35 USC § 103

19. Claim 78 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US '647 B1) as applied to claim 77 above, and further in view of Ohashi (US 6,184,143 B1).

Li differs in failing to teach wherein said reacting step comprises reacting said hydrogen with a selection comprising dimethylsilane, trimethylsilane, tetramethylsilane, pentamethyldisilane, and combinations thereof.

Ohashi teaches, "A silicon oxide film formed . . . by the combination of a silane gas (SiH_4) and hydrogen peroxide (H_2O_2) under reduced pressure, to absorb to the surface of a substrate to form a film, can also be given as an example of the fluid insulating film. Here, a silane gas is exemplified as a raw material gas for the formation of a silanol, but methylsilane (dimethylsilane, trimethylsilane or the like) or ethylsilane (diethylsilane, triethylsilane or the like) having, as a substituent for a hydrogen group (--H), an alkyl group such as methyl (--CH_3) or ethyl (--C_2H_5) may be used" (column 4, lines 48-61).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Li by using Ohashi's method of reacting hydrogen peroxide with a gas such as dimethylsilane, trimethylsilane or the like for the purpose of making a fluid insulating layer that does not affect the reliability of the semiconductor device (see Ohashi, column 4, lines 28-42).

Allowable Subject Matter

20. Claims 59-65 are allowed.

21. The following is a statement of reasons for the indication of allowable subject matter: As to claims 59-65, the prior art of record taken alone or in combination fail to suggest, teach, or render obvious a method of forming oxide over a transistor gate and over a substrate extending laterally from under said gate, comprising: stopping said removal of a portion of said insulation with said second oxide, in combination with the rest of the limitations of the said claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 1765

ltue

December 9, 2004

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER